CLAIMS

1. A device for transferring data between two asynchronous systems, comprising:

a write pointer register in a first system for writing data;

a read pointer register in a second system for reading data;

a buffer memory connected between the first and second systems;

a first shadow register located in said first system and connected to said write pointer register to receive contents of said write pointer register;

a second shadow register located in said second system and connected to said read pointer register to receive contents of said read pointer register;

a third shadow register located in said first system and connected to said second shadow register to receive contents of said second shadow register;

a fourth shadow register located in said second system and connected to said first shadow register to receive contents of said first shadow register;

a first compare circuit comparing the contents of said write pointer register with the contents of said third shadow register in order to authorize writes to said buffer memory; and

a second compare circuit comparing of the contents of said read pointer register with the contents of said fourth shadow register in order to authorize reads in said buffer memory.

2. A device according to claim 1, further comprising a handshake circuit controlling successively the transfer of the contents of said write pointer register to said first shadow register, then to said fourth shadow register.

3. A device according to claim 1, further comprising a handshake circuit controlling successively the transfer of the contents of said read pointer register to said second shadow register, then to said third shadow register.

4. A device according to claim 3 wherein said handshake circuit comprises a loop of registers or flip-flops combined with a reverser element in order to allow the circulation of a switching state on the loop, said state being used successively as a flag for said first system and a flag for said second receive system.

5. A device according to claim 4 wherein, in said first system, said handshake circuit comprises:

a first flip-flop having an input and an output, said input receiving the flag of the second system;

a second flip-flop having an input and an output, said input receiving the output of said first flip-flop;

a first multiplexer having a first reverser input connected to the output of said second flip-flop and a second non-reverser input receiving the flag transmitted to the second system;

a third flip-flop having an input connected to said output of said multiplexer and an output generating said flag transmitted to the second system; and

a first XOR gate having a first input connected to the output of said third flip-flop and a second input connected to the output of said multiplexer.

6. A device according to claim 5 wherein said first system comprises:

a second multiplexer controlled by said first XOR gate and allowing transfer between said second shadow register and said third shadow register; and

a third multiplexer allowing transfers between said write pointer register and said first shadow register.

7. A device according to claim 5 wherein, in said second system, said handshake circuit comprises:

a fourth flip-flop having an input and an output, said input receiving the flag of said first system;

a fifth flip-flop having an input and an output, said input receiving the output of said fourth flip-flop;

a sixth flip-flop having an input connected to said output of said fifth flip-flop and an output generating the flag transmitted to said first system; and

a second XOR gate having a first input connected to the output of said fifth flip-flop and a second input connected to the output of said sixth flip-flop.

8. A device according to claim 7 wherein said second system comprises:

a second multiplexer controlled by said second XOR gate and allowing transfer between said first shadow register and said fourth shadow register; and

a third multiplexer allowing transfers between said read pointer register and said second shadow register.

9. A device according to claim 1 wherein said buffer memory is a FIFO memory realized by a dual port memory.

10. A device according to claim 9 wherein said first and second systems are integrated in the same semiconductor product.

11. A device for transferring data between asynchronous first and second systems, comprising:

a write pointer register in the first system for writing data;

a read pointer register in a second system for reading data;

a buffer memory connected between the first and second systems;

a first shadow register located in the first system and connected to the write pointer register to receive contents of the write pointer register;

a second shadow register located in the second system and connected to the read pointer register to receive contents of the read pointer register;

a third shadow register located in the first system and connected to the second shadow register to receive contents of the second shadow register; and

a first compare circuit comparing the contents of the write pointer register with the contents of the third shadow register in order to authorize writes to the buffer memory.

12. The device of claim 11, further comprising:

a fourth shadow register located in the second system and connected to the first shadow register to receive contents of the first shadow register; and

a handshake circuit controlling successively the transfer of the contents of the write pointer register to the first shadow register, then to the fourth shadow register.

13. The device of claim 12 wherein the handshake circuit comprises a loop of registers or flip-flops combined with a reverser element in order to allow the circulation of a switching state on the loop, the state being used successively as a flag for the first system and a flag for the second receive system.

14. The device of claim 12 wherein the handshake circuit comprises:

a first multiplexer having first and second inputs and an output;

a first flip-flop having an input connected to the output of the first multiplexer and an output generating a first flag that is transmitted to the second system;

a first logic gate having a first input connected to the output of the first flip-flop, a second input connected to the output of the first multiplexer, and an output connected to the second input of the first multiplexer;

a second flip-flop having an input connected to the output of the first flip-flop and an output generating a second flag that is transmitted to the first system and

a second logic gate having a first input connected to the output of the first flip-flop, a second input connected to the output of the second flip-flop, and an output

that controls the transfer of the contents of the first shadow register to the fourth shadow register and controls the transfer of the contents of the read pointer register to the second shadow register.

15. The device of claim 14 wherein the first system comprises:

a second multiplexer controlled by the first logic gate and allowing transfer between the second shadow register and the third shadow register; and

a third multiplexer allowing transfers between the write pointer register and the first shadow register.

16. The device of claim 15 wherein the second system comprises:

a fourth multiplexer connected to the output of the second logic gate and allowing transfer between the first shadow register and the fourth shadow register; and

a fifth multiplexer connected to the output of the second logic gate and allowing transfers between the read pointer register and the second shadow register.

17. The device of claim 14 wherein the handshake circuit further comprises:

a third flip-flop having an input and an output, the input being connected to the output of the second flip-flop;

a fourth flip-flop having an input connected to the output of the third flip-flop, and an output connected to the first input of the first multiplexer;

a fifth flip-flop having an input and an output, the input being connected to the output of the first flip-flop; and

a sixth flip-flop having an input connected to the output of the fifth flip-flop and an output connected to the input of the second flip-flop.

18. The device of claim 11 wherein the buffer memory is a FIFO memory realized by a dual port memory.

19. The device of claim 11 wherein the first and second systems are integrated in the same semiconductor product.

20. A method of transferring data between asynchronous first and second systems, the first system including a write pointer register and the second system including a read pointer register, the method comprising:

transmitting contents of the write pointer register into a first shadow register in the first system;

transmitting contents of the read pointer register into a second shadow register in the second system;

transmitting contents of the second shadow register into a third shadow register in the first system;

comparing the contents of the write pointer register with the contents of the third shadow register; and

authorizing writes to a buffer memory connected between the first and second systems based on results of the comparing step.

21. The method of claim 20, further comprising:

creating a first flag that controls the step of transmitting the contents of the read pointer register into the second shadow register;

inverting the first flag to create a second flag that controls the steps of transmitting the contents of the write pointer register into the first shadow register and transmitting the contents of the second shadow register into the third shadow register.

22. The method of claim 21, further comprising:

transmitting contents of the first shadow register into a fourth shadow register in the second system; and

controlling, using the first flag, the step of transmitting the contents of the first shadow register into the fourth shadow register.